

**Serial No. 09/546,833****PATENT****Docket No. RAL920000042US1****REMARKS**

This amendment is in response to the Office Action mailed July 31, 2003.

Claims 1 and 5 are rejected under 35 USC 102(e) as being anticipated by Hassell et al. (U.S. Patent Number 6,208,650 B1). On page 2 of the Office Action the Examiner seems to argue that Hassell et al. discloses all the elements of claim 1 including data for identifying a beginning of a processing sequence for the egress processor.

Applicants respectfully disagree with the Examiner's position that the reference shows this feature of applicants' invention. In Hassell et al. the input processor forms a pointer which points to the address in memory whereat the payload in the frame is stored. This has always been the traditional way of handling input data. The starting instruction which the second processor used to process the information stored in memory is never included in the header provided by the input processor, as is required in applicants' claim 1. In applicants' claim 1 the Ingress processor generates the header and in that header indicates the starting point in the instruction set for the egress scheduler. By so doing information processed by the ingress processor is not redone by the egress processor. Even though applicants believe the claims as written initially distinguish over the Examiner's cited reference the claim is amended to make the point clearer by stating the contents in the header relates to the beginning of an instruction processing sequence. The claim as now amended clearly distinguishes over the art of record.

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Regarding claim 5 the Examiner argues that it is inherent in Hassell that multiple frames would have to be transmitted through multiple ports if the frame contains multiple data. Applicants respectfully disagree with the Examiner and contends inherent characteristics mean the processor has the capability of recognizing this feature. However, a review of the Hassell reference discloses or indicates no reason why the processor would ever recognize multiple frames for multiple ports if this features was not specifically built into the processor. Because Hassell et al. is silent regarding multiple frames and this feature is not inherent in processors (applicants know of several processors that cannot handle multicast frames) then claim 5 is not anticipated.

In addition, claim 5 depends on claim 1 and for the reasons set forth above it too is patentable over the art of record.

The Examiner indicates claims 8-18 are allowed and are not discussed further in this amendment. The Examiner indicates claims 3, 4, 6 and 7 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, claims 3, 4, 6 and 7 have been rewritten in independent form and are now in a condition for allowance which is respectfully solicited.

The newly added claims are also patentable over the art of record for reasons set forth above.

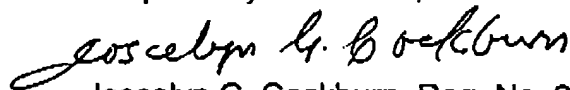
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It is believed that the present amendment answers all the issues raised by the Examiner. Reconsideration is hereby requested and an early allowance of all the claims is solicited.

Respectfully Submitted,



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